Last time

Finished measurements in 3-Phase rectifier lab

Today: Steady state behavior for L, C containing circuits.

Many of the circuits we will be interested in will contain inductors and capacitors and be driven by periodic (but not sinusoidal) inputs. There will often be a settling down interval of time after which the circuit will reach steady state.

* Steady state differs from static equilibrium as i, V will still vary w/ time. This variation will be periodic w/ the same period as the input signal

* Fourier series doesn't help. w/o a sinusoidal input Fourier series will give an output, but it will not provide insight

But for ideal capacitors & inductors the equation relating current and voltage provide a means to a useful simplification

For an ideal Cap, Inductor (i.e. no series resistance)

 

? ?

Eq: Ans next page.

$$\frac{dV}{dt} = \frac{1}{C} i \qquad \text{Eq } (1)$$

$$\frac{di}{dt} = \frac{1}{L} V \qquad \text{Eq } (2)$$

1st focus on this

in steady state

$V(t)$ = periodic f^n

$i(t)$ = periodic f^n

notice that if we integrate Eq (1) w/rt for 1 period, T.

$$\int_0^T \frac{dv}{dt}\, dt = \frac{1}{C} \int_0^T i(t)\, dt$$

$$V(T) - V(0) = \frac{1}{C} \int_0^T i(t)\, dt$$

but since $V(t)$ is periodic $V(T) = V(0) \Rightarrow V(T) - V(0) = 0$

$$0 = \frac{1}{C} \int_0^T i(t)\, dt$$

recall def: of

$$\langle i \rangle = \frac{1}{T} \int_0^T i(t)\, dt$$

so that

$$0 = \frac{T}{C} \langle i \rangle$$

or

$\langle i \rangle = 0$ so that the capacitor is not, on average, charging. ~~the area~~

current through capacitor

Equivalently the area under the current curve for 1 period is zero.

By similar arguments

Eq (2) $\frac{di}{dt} = \frac{1}{L} V$ in steady state

implies

$$\langle V \rangle = 0$$

voltage across inductor